UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,464	01/27/2004	David Lewis	174/285	3178

36981	7590	09/06/2006		

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EXAMINER
BONURA, TIMOTHY M

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/766,464	LEWIS ET AL.
	Examiner	Art Unit	
	Tim Bonura	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2006*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

　　4a) Of the above claim(s) *29-36,52 and 53* is/are withdrawn from consideration.

5)☐ Claim(s) *27 and 28* is/are allowed.

6)☐ Claim(s) *1-3,16-23,37-40 and 42-51* is/are rejected.

7)☐ Claim(s) *4-15, 24-26, and 41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All   b)☐ Some * c)☐ None of:

　　　1.☐ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
　　Paper No(s)/Mail Date *10/12/04 & 3/10/06*.

4) ☐ Interview Summary (PTO-413)
　　Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2.   The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

     1.   Determining the scope and contents of the prior art.
     2.   Ascertaining the differences between the prior art and the claims at issue.
     3.   Resolving the level of ordinary skill in the pertinent art.
     4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

3.   Claims 1-3, 16-23, 37-40, and 42-51 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Ding, et al, U.S. Patent Number 7,058,800 and further in view of Walker, et

al, U.S. Patent Number 6,845,472.

4.   Regarding claim 1:

a.   Regarding the limitation of "a memory in which the configuration data and error

check data associated with the configuration data is stored," Ding discloses a system

with a programmable logic circuit with a memory for storing data, which can be extracted

for verification. (Lines 51-56 of Column 1). Ding does not disclose a system wherein

configuration data is stored in the memory. However, Walker discloses a system with

error checking using ECC in memory area with extended period of time between

accesses, such as a memory control device. (Lines 30-35 and Lines 60-65 of Column

6). It would have been one of ordinary skill at the time of the invention to combine the

PLD of Ding with the error checking of Walker. One would have been inclined because Walker discloses a system with an advantage of check error before accumulation can occur and error becoming uncorrectable. (Lines 30-35 of Column 6).

b.   Regarding the limitation of "error correction circuitry coupled to at least some of the memory to analyze the configuration data stored in the memory to determine if any values have changed after initial configuration of the memory and to correct any values that have changed," Walker discloses a system wherein error are checked and corrected if found in memory. (Lines 39-46 of Column 6).

5.   Regarding claim 2:

c.   Regarding the limitation of "read from the memory a portion of the configuration data and an associated portion of the error check data," Walker disclose the ability to error check any piece of memory in a computer sub-system. (Lines 35-38 of Column 6).

d.   Regarding the limitation of "apply an error correcting code on the portion of the configuration data and the associated portion of the error check data to determine whether at least one bit in the portion of the configuration data has an error and to correct the at least one bit that has the error," Walker discloses a system that uses ECC bit checking to detect and correct errors. (Lines 35-41 of Column 6).

6.   Regarding claim 3, Walker discloses a system with a cleaning procedure that uses ECC to check data in a sub-set of memory. (Lines 34-41 of Column 6).

7.   Regarding claim 16:

e.   Regarding the limitation of "processing circuitry," Ding discloses a program logic circuit. (Lines 51-52 of Column 1).

f.   Regarding the limitation of "a memory coupled to the processing circuitry," Ding discloses a program logic circuit with memory for storing data. (Lines 51-54 of Column 1).

g.   Regarding the limitation of "a programmable logic device as defined in claim 1 coupled to the processing circuitry and the memory," Ding discloses a program logic circuit with memory contained within the circuitry for storing program data in rows and columns. (Lines 51-52 of Column 1).

8.   Regarding claim 17, Ding discloses a system of interconnected PLD on array grid. (Lines 40-55 of Column 2).

9.   Regarding claim 18, Ding discloses a system of interconnected PLD on array grid, connected to the PLD are EEPROM cells. (Lines 40-55 of Column 2).

10.   Regarding claim 19, Ding discloses a system of interconnected PLD on array grid with a plurality of logic array blocks. (Lines 40-55 of Column 2).

11.   Regarding claim 20:

h.   Regarding the limitation of "a memory in which the configuration data and error check data associated with the configuration data is stored," Ding discloses a system with a programmable logic circuit with a memory for storing data, which can be extracted for verification. (Lines 51-56 of Column 1). Ding also discloses storing data in rows and columns. (Lines 45-50 of Column 20. Ding does not disclose a system wherein configuration data is stored in the memory. However, Walker discloses a system with error checking using ECC in memory area with extended period of time between accesses, such as a memory control device. (Lines 30-35 and Lines 60-65 of Column 6). It would have been one of ordinary skill at the time of the invention to combine the PLD of Ding with the error checking of Walker. One would have been inclined because

Walker discloses a system with an advantage of check error before accumulation can occur and error becoming uncorrectable. (Lines 30-35 of Column 6).

i.   Regarding the limitation of "at least on scrubber coupled to the memory," Walker discloses a system with a cleaning procedure for checking memory errors. (Lines 30-32 of Column 6).

j.   Regarding the limitation of "read from the memory a portion of the configuration data and an associated portion of the error check data," Walker disclose the ability to error check any piece of memory in a computer sub-system. (Lines 35-38 of Column 6).

k.   Regarding the limitation of "apply an error correcting code on the portion of the configuration data and the associated portion of the error check data to determine whether at least one bit in the portion of the configuration data has an error and to correct the at least one bit that has the error," Walker discloses a system that uses ECC bit checking to detect and correct errors. (Lines 35-41 of Column 6).

12.   Regarding claim 21, Walker discloses a system with a cleaning procedure that uses ECC to check data in a sub-set of memory. (Lines 34-41 of Column 6).

13.   Regarding claim 22, Walker discloses a system with a cleaning procedure that uses ECC to check data in a sub-set of memory. (Lines 34-41 of Column 6).

14.   Regarding claim 23, Walker disclose a system that using ECC codes. (Lines 39-41 of Column 6).

15.   Regarding claim 37:

l.   Regarding the limitation of "generating and storing error check data associated with the configuration data in a memory," Ding discloses a system with a programmable logic circuit with a memory for storing data, which can be extracted for verification. (Lines 51-56 of Column 1). Ding also discloses storing data in rows and columns.

(Lines 45-50 of Column 20. Ding does not disclose a system wherein configuration data is stored in the memory. However, Walker discloses a system with error checking using ECC in memory area with extended period of time between accesses, such as a memory control device. (Lines 30-35 and Lines 60-65 of Column 6). It would have been one of ordinary skill at the time of the invention to combine the PLD of Ding with the error checking of Walker. One would have been inclined because Walker discloses a system with an advantage of check error before accumulation can occur and error becoming uncorrectable. (Lines 30-35 of Column 6).

m.   Regarding the limitation of "reading a portion of the configuration data and an associated portion of the error check data," Walker discloses a system in which a portion of memory is read for error checking with a cleansing procedure. (Lines 30-32 of Column 6).

n.   Regarding the limitation of "determining if an error has occurred based on the portion of the configuration data and the associated portion of the error check data," Walker discloses a system in which errors are recorded in corrected. (Lines 44-46 of Column 6).

o.   Regarding the limitation of "correcting the portion of the configuration data in response to the determining," Walker discloses a system in which errors are recorded in corrected. (Lines 44-46 of Column 6).

16.   Regarding claim 38, Ding discloses a system in which the data is stored with rows and columns of memory cells. (Lines 46-50 of Column 2).

17.   Regarding claim 39, Ding discloses a system in which the data is stored with rows and columns of memory cells. (Lines 46-50 of Column 2).

18.   Regarding claim 40, Ding discloses a system in which the data is stored with rows and columns of memory cells. (Lines 46-50 of Column 2).

19.   Regarding claim 42, Walker disclose a system that using ECC codes. (Lines 39-41 of Column 6).

20.   Regarding claim 43, Walker disclose a system that using ECC codes. (Lines 39-41 of Column 6).

21.   Regarding claim 44, Walker discloses a system with error checking using ECC in memory area with extended period of time between accesses, such as a memory control device. (Lines 30-35 and Lines 60-65 of Column 6). Walker discloses a system in which errors are recorded in corrected. (Lines 44-46 of Column 6).

22.   Regarding claim 45:

        p.   Regarding the limitation of "generating and storing a parity bit associated with each representative row and each representative column of memory cell in which the configuration data is stored," Ding discloses a system with a programmable logic circuit with a memory for storing data, which can be extracted for verification. (Lines 51-56 of Column 1). Ding also discloses storing data in rows and columns. (Lines 45-50 of Column 20. Ding does not disclose a system wherein configuration data is stored in the memory. However, Walker discloses a system with error checking using ECC in memory area with extended period of time between accesses, such as a memory control device. (Lines 30-35 and Lines 60-65 of Column 6). It would have been one of ordinary skill at the time of the invention to combine the PLD of Ding with the error checking of Walker. One would have been inclined because Walker discloses a system with an advantage of check error before accumulation can occur and error becoming uncorrectable. (Lines 30-35 of Column 6).

q.   Regarding the limitation of "computing a first parity on a given representative column of memory cells," Ding discloses verifying data in N-2 register using the N-1 registers as verification. (Lines 60-67 of Column 7).

r.   Regarding the limitation of "computing a second parity on a given representative column of memory cells," Ding discloses verifying data in N-1 register using the N registers as verification. (Lines 60-67 of Column 7).

s.   Regarding the limitation of "determining if an error has occurred in a cell in a given representative row and the given representative column based on the first parity and the second parity," Ding discloses a system in which errors in data can be verified in memory elements. (Lines 26-65 of Column 3).

t.   Regarding the limitation of "correcting the portion of the configuration data in response to the determining," Walker discloses a system in which errors are recorded in corrected. (Lines 44-46 of Column 6).

23.   Regarding claim 46, Walker discloses a system with a parity bit of even and odd for in column. (Lines 12-30 of Column 5).

24.   Regarding claim 47, Walker discloses a system wherein parity bits can be used to correct errors in data. (Lines 32-37 of Column 5).

25.   Regarding claim 48, Walker discloses a system wherein parity bits can be used to correct errors in data. (Lines 32-37 of Column 5).

26.   Regarding claim 49:

u.   Regarding the limitation of "generating and storing a parity bit associated with each representative row and each representative column of memory cell in which the configuration data is stored," Ding discloses a system with a programmable logic circuit with a memory for storing data, which can be extracted for verification. (Lines 51-56 of

Column 1). Ding also discloses storing data in rows and columns. (Lines 45-50 of Column 20. Ding does not disclose a system wherein configuration data is stored in the memory. However, Walker discloses a system with error checking using ECC in memory area with extended period of time between accesses, such as a memory control device. (Lines 30-35 and Lines 60-65 of Column 6). It would have been one of ordinary skill at the time of the invention to combine the PLD of Ding with the error checking of Walker. One would have been inclined because Walker discloses a system with an advantage of check error before accumulation can occur and error becoming uncorrectable. (Lines 30-35 of Column 6).

v.   Regarding the limitation of "computing a first parity on a given representative column of memory cells," Ding discloses verifying data in N-2 register using the N-1 registers as verification. (Lines 60-67 of Column 7).

w.   Regarding the limitation of "computing a second parity on a given representative column of memory cells," Ding discloses verifying data in N-1 register using the N registers as verification. (Lines 60-67 of Column 7).

x.   Regarding the limitation of "generating a correct value for the data in one cell based on the first parity the second parity and data in one cell," Walker discloses a system in which errors are recorded in corrected. (Lines 44-46 of Column 6).

27.   Regarding claim 50, Walker discloses a system with a parity bit of even and odd for in column. (Lines 12-30 of Column 5).

28.   Regarding claim 51, Walker discloses a system wherein parity bits can be used to correct errors in data. (Lines 32-37 of Column 5).

Allowable Subject Matter

29.   Claims 27-28 are allowed.

30.   The following is an examiner's statement of reasons for allowance the prior art of record does not teach the limitation of "a memory array of representative rows and representative columns of cells in which the configuration data and error check data associated with the configuration data are stored; first circuitry having an input operative to receive data from each cell in a representative row of the array and an output, the first circuitry generating a first parity for the data in the representative row at the output; second circuitry having an input operative to receive data from each cell in a representative column of the array and an output, the second circuitry generating a second parity for the data in the representative column at the output; third circuitry having a first input operative to receive the output of the first circuitry, having a second input operative to receive the output of the second circuitry, and an output, the third circuitry sending a signal at the output indicative of whether an error has occurred in a cell in the representative row and the representative column based on the first parity and the second parity; and fourth circuitry having a first input operative to receive the output of the third circuitry, a second input operative to receive data from the cell in the representative row and the representative column, and an output, the fourth circuitry sending a signal at the output having a correct value."

31.   Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

32.   Claims 4-15, 24-26, and 41 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

33.   The following is a statement of reasons for the indication of allowable subject matter: Regarding claim 4, the prior art of record does not teach the limitation of "the configuration data is stored in an array of representative rows and representative columns of cells, each cell storing one bit of the configuration data; and the error check data is stored in a last representative column of cells and a last representative row of cells in the array, each cell storing one bit of the error check data."

34.   Regarding claim 10, the prior art of record does not teach the limitation of "each bit of the configuration data is stored in a first cell, a second cell, and a third cell in the memory."

35.   Regarding claim 14, the prior art of record does not teach the limitation of "a resistive element coupled to an output of the error correction circuitry; and a capacitive load coupled to the resistive element, wherein the resistive element and the capacitive load are operative to reduce static hazards associated with the error correction circuitry."

36.   Regarding claim 24, the prior art of record does not teach the limitation of "a memory array of representative rows and representative columns of cells in which the configuration data and error check data associated with the configuration data are stored; first circuitry having an input operative to receive data from each cell in a representative row of the array and an output, the first circuitry generating a first parity for the data in the representative row at the output; second circuitry having an input operative to receive data from each cell in a representative column of the array and an output, the second circuitry generating a second parity for the data in the representative column at the output; third circuitry having a first input operative to receive the output of the first circuitry, having a second input operative to receive the output of the

second circuitry, and an output, the third circuitry sending a signal at the output indicative of

whether an error has occurred in a cell in the representative row and the representative column

based on the first parity and the second parity; and fourth circuitry having a first input operative

to receive the output of the third circuitry, a second input operative to receive data from the cell

in the representative row and the representative column, and an output, the fourth circuitry

sending a signal at the output having a correct value."

37.   Regarding claim 41, the prior art of record does not teach the limitation of "the portion of

the configuration data is at least two partial representative columns of cells in the memory that

are physically non-contiguous."
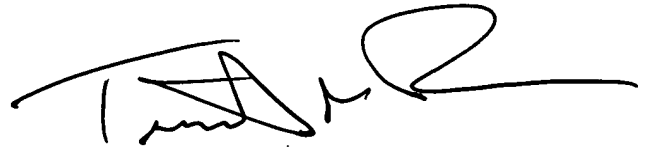

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner

should be directed to Tim Bonura whose telephone number is 571-272-3654. The examiner

can normally be reached on M-F 9:30AM - 6:00PM (Eastern).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Scott Baderman can be reached on 571-272-3644. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private

PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you

would like assistance from a USPTO Customer Service Representative or access to the

automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tim Bonura
Examiner
Art Unit 2114